In The Specification:

Please amend the paragraphs [0013], [0028] and [0033] as follows:

[0013] The present invention provides a fabrication method for a memory device. This method comprises forming a patterned mask layer on a substrate, wherein this mask layer is a photoresist layer, a polysilicon layer or a dielectric layer (for example, silicon nitride or silicon oxide type of dielectric material). Thereafter, using the mask layer as an ion implantation mask, a first ion implantation process is performed to form a shallow doped region in the substrate not covered by the mask layer. A linear layer is then formed on the surface of the mask layer, wherein the liner layer is formed by, for example, plasma enhanced chemical vapor deposition and the liner layer is, for example, a ~~high molecular weight~~ polymer liner layer. A point that is worth noting is that if the liner layer formed on the surface of the mask layer is a ~~high molecular weight~~ polymer layer, the liner layer can be reworked even deviation occurs in the critical dimension of the liner layer. A second ion implantation process is performed to form a deep doped region in the substrate not covered by the liner layer and the mask layer, using the liner layer and the mask layer as an implantation mask, wherein the shallow doped region and the deep doped region together form a bit line of a memory device. The mask layer and the liner layer are then removed, followed by forming a gate oxide layer on the surface of the substrate and a gate on the gate oxide layer.

[0028] Referring to Figure 2C, a liner layer 112 with a pre-determined thickness is formed on the surface of the mask layer 106, wherein the liner layer 112 is formed by, for example, plasma enhanced chemical vapor deposition. A material for the liner layer 112 is, for example, a ~~high molecular weight~~ polymer material. A point that is worth noting is that if the liner layer 112 is a ~~high molecular weight~~ polymer layer, the liner layer 112 can be reworked directly even deviation occurs in the critical dimension of the liner layer.

[0033] Continuing to Figure 2E, the liner layer 112 and the mask layer 106 are removed. If the mask layer 106 is a photoresist material and the liner layer 112 is a ~~high molecular weight~~ polymer material, the photoresist material mask layer 106 (including anti-reflection layer 104) and the liner layer 112 can be removed concurrently. After this, the pad oxide layer 102 is removed to expose the surface of the substrate 100.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 9-15 and 25-36 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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